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AAP Gen 7 (TO-240AA) **Power Modules Schottky Rectifier, 220 A**



AAP Gen 7 (TO-240AA)

PRIMARY CHARACTERISTICS			
I _{F(AV)}	220 A		
V _R	30 V		
Package	AAP Gen 7 (TO-240AA)		
Circuit configuration	Two diodes doubler circuit		

MECHANICAL DESCRIPTION

The AAP Gen 7, new generation of ADD-A-PAK module, combines the excellent thermal performances obtained by the usage of exposed direct bonded copper substrate, with advanced compact simple package solution and simplified internal structure with minimized number of interfaces.

FEATURES

- 150 °C T_J operation
- · Low forward voltage drop
- High frequency operation
- Low thermal resistance
- UL approved file E78996
- · Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

BENEFITS

- · Excellent thermal performances obtained by the usage of exposed direct bonded copper substrate
- High surge capability
- · Easy mounting on heatsink

ELECTRICAL DESCRIPTION / APPLICATIONS

The VS-VSKDS440.. Schottky rectifier doubler has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 150 °C junction temperature.

Typical applications are in high current switching power supplies, plating power supplies, UPS systems, converters, freewheeling diodes, welding, and reverse battery protection.

MAJOR RATINGS AND CHARACTERISTICS					
SYMBOL	CHARACTERISTICS	CHARACTERISTICS VALUES			
I _{F(AV)}	Rectangular waveform	220	A		
V _{RRM}		30	V		
I _{FSM}	t _p = 5 μs sine	p = 5 μs sine 27 000			
V _F	110 A _{pk} , T _J = 125 °C	0.43	V		
TJ	Range	-55 to +150	°C		

VOLTAGE RATINGS			
PARAMETER	SYMBOL	VS-VSKDS440/030	UNITS
Maximum DC reverse voltage	V _R	30	
Maximum working peak reverse voltage	V _{RWM}		

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COMPLIANT

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ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average forward current	I _{F(AV)}	$I_{F(AV)}$ 50 % duty cycle at T _C = 97 °C, rectangular waveform		220	
Maximum peak one cycle	ESM	5 μs sine or 3 μs rect. pulse	Following any rated load condition and with rated V _{RRM} applied	27 000	А
non-repetitive surge current		10 ms sine or 6 ms rect. pulse		3000	
Non-repetitive avalanche energy	E _{AS}	T _J = 25 °C, I _{AS} = 20 A, L = 1 mH		198	mJ
Repetitive avalanche current	I _{AR}	Current decaying linearly to zero in 1 μ s Frequency limited by T _J maximum V _A = 1.5 x V _R typical 44		А	

ELECTRICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum forward voltage drop	V _{FM}	220 A	T _J = 25 °C	0.68	v
		440 A		1.0	
		220 A	T _J = 125 °C	0.61	
		440 A		0.93	
	I _{RM}	T _J = 25 °C	V _R = Rated V _R	20	mA
Maximum reverse leakage current		T _J = 125 °C		1120	ША
Maximum junction capacitance	CT	$V_{R} = 5 V_{DC}$ (test signal range 100 kHz to 1 MHz), 25 °C		14 800	pF
Typical series inductance	L _S	Measured lead to lead 5 mm from package body		5.0	nH
Maximum voltage rate of change	dV/dt	Rated V _R		10 000	V/µs
Maximum RMS insulation voltage	V _{INS}	50 Hz		3000 (1 min) 3600 (1 s)	V

THERMAL - MECHANICAL SPECIFICATIONS						
PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS	
Maximum junction and storage temperature range		T _J , T _{Stg}		-55 to +150	°C	
Maximum thermal resistance, junction to case per leg		R _{thJC} DC operation		0.26	°C/W	
Typical thermal resistance, case to heatsink per module		R _{thCS}		0.1	- 0/00	
Annual in the surface to				75	g	
Approximate weight			2.7	oz.		
Mounting torque ± 10 %	to heatsink		A mounting compound is recommended and the torque should be rechecked after a period of 3 h to allow for the	4	Nm	
	busbar		spread of the compound.	3	11111	
Case style			JEDEC®	TO-240AA co	ompatible	



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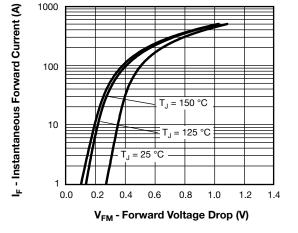


Fig. 1 - Maximum Forward Voltage Drop Characteristics

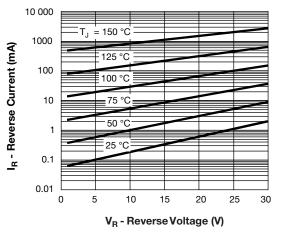


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

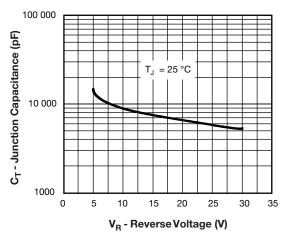


Fig. 3 - Typical Junction Capacitance vs.Reverse Voltage

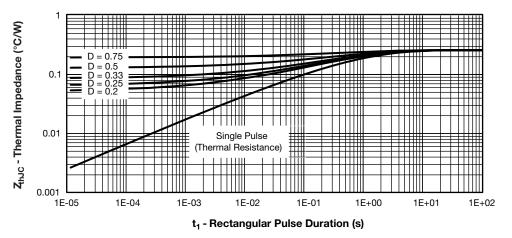
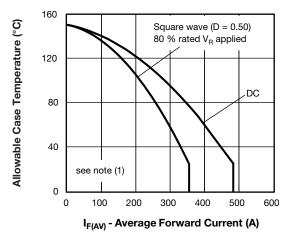


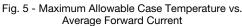
Fig. 4 - Maximum Thermal Impedance ZthJC Characteristics

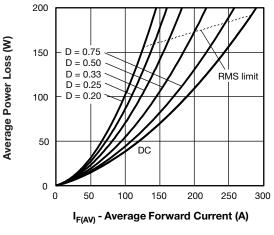
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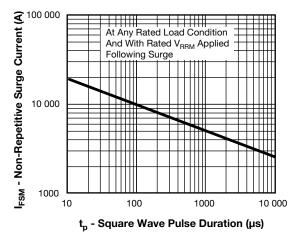


Fig. 7 - Maximum Non-Repetitive Surge Current

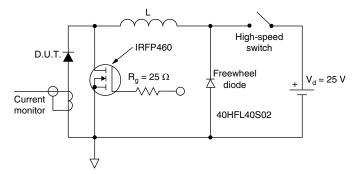


Fig. 8 - Unclamped Inductive Test Circuit

Note

 Pd_{REV} = inverse power loss = $V_{R1} \times I_R (1 - D)$; I_R at V_{R1} = 80 % rated V_R

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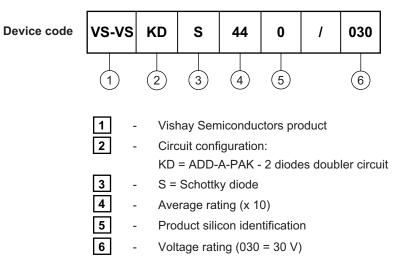
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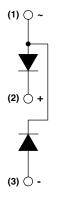
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ORDERING INFORMATION TABLE



CIRCUIT CONFIGURATION



LINKS TO RELATED DOCUMENTS			
Dimensions	www.vishay.com/doc?95369		

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ADD-A-PAK Generation VII - Diode

DIMENSIONS in millimeters (inches)





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