![SYC SEMICONDUCTORES Y COMPONENTES]

CD4069, CD4069-SMD
Inverter Circuits

General Description

The CD4069UB consists of six inverter circuits and is man-ufactured using complementary MOS (CMOS) to achieve wide power supply operating range, low power consump-tion, high noise immunity, and symmetric controlled rise and fall times.

This device is intended for all general purpose inverter applications where the special characteristics of the MM74C901, MM74C907, and CD4049A Hex Inverter/Buff-ers are not required. In those applications requiring larger noise immunity the MM74C14 or MM74C914 Hex Schmitt Trigger is suggested.

All inputs are protected from damage due to static dis-charge by diode clamps to V_{DD} and V_{SS}.

Features
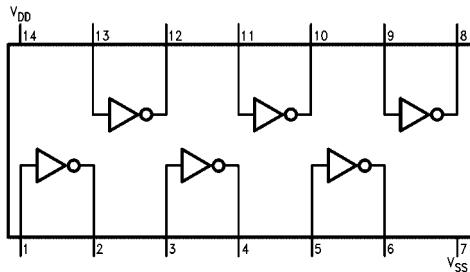
■ Wide supply voltage range: 3.0V to 15V
■ High noise immunity: 0.45 V_{DD} typ.
■ Low power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS
■ Equivalent to MM74C04

Ordering Code:
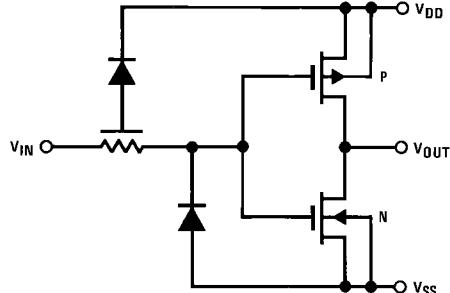
Order Number	Package Number	Package Description
CD4069UBCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4069UBCSJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4069UBCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix "X" to the ordering code.

Connection Diagram

Schematic Diagram

SYC SEMICONDUCTORES Y COMPONENTES

Absolute Maximum Ratings(Note 1)

(Note 2)

DC Supply Voltage (V_{DD})	−0.5V to +18 V_{DC}
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3V to 15V_{DC}
Input Voltage (V_{IN})	0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)	−55°C to +125°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and Electrical Characteristics table provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	−55°C Min	−55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Units
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		0.25			0.25		7.5	
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		0.5			0.5		15	µA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		1.0			1.0		30	
V_{OL}	LOW Level Output Voltage	$|I_O| < 1$ µA								
		V_{DD} = 5V		0.05		0	0.05		0.05	
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	
V_{OH}	HIGH Level Output Voltage	$|I_O| < 1$ µA								
		V_{DD} = 5V	4.95		4.95	5		4.95		
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		
V_{IL}	LOW Level Input Voltage	$|I_O| < 1$ µA								
		V_{DD} = 5V, V_O = 4.5V		1.0			1.0		1.0	
		V_{DD} = 10V, V_O = 9V		2.0			2.0		2.0	V
		V_{DD} = 15V, V_O = 13.5V		3.0			3.0		3.0	
V_{IH}	HIGH Level Input Voltage	$|I_O| < 1$ µA								
		V_{DD} = 5V, V_O = 0.5V	4.0		4.0			4.0		
		V_{DD} = 10V, V_O = 1V	8.0		8.0			8.0		V
		V_{DD} = 15V, V_O = 1.5V	12.0		12.0			12.0		
I_{OL}	LOW Level Output Current (Note 4)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		
I_{OH}	HIGH Level Output Current (Note 4)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	

Note 3: V_{SS} = 0V unless otherwise specified.

Note 4: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 5)
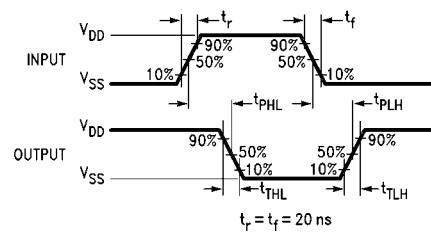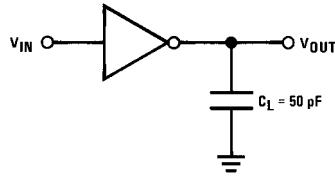
$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, t_r and $t_f \leq 20$ ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL} or t_{PLH}	Propagation Delay Time from Input to Output	$V_{DD} = 5V$		50	90	ns
		$V_{DD} = 10V$		30	60	
		$V_{DD} = 15V$		25	50	
t_{THL} or t_{TLH}	Transition Time	$V_{DD} = 5V$		80	150	ns
		$V_{DD} = 10V$		50	100	
		$V_{DD} = 15V$		40	80	
C_{IN}	Average Input Capacitance	Any Gate		6	15	pF
C_{PD}	Power Dissipation Capacitance	Any Gate (Note 6)		12		pF

**Note 5:** AC Parameters are guaranteed by DC correlated testing.
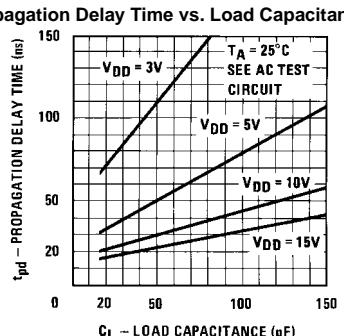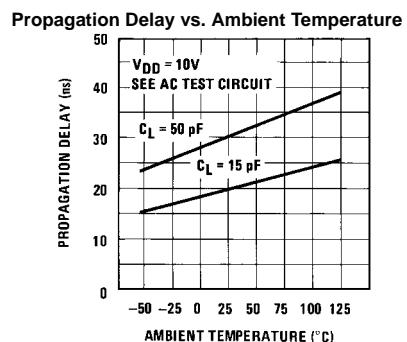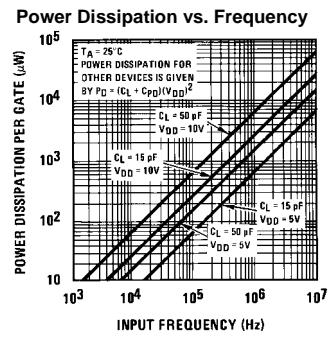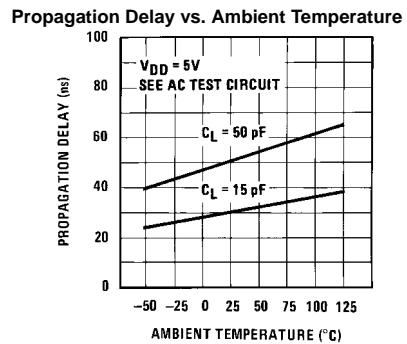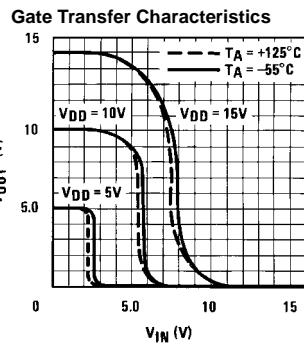
Note 6: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see Family Characteristics application note— AN-90.

AC Test Circuits and Switching Time Waveforms

Typical Performance Characteristics
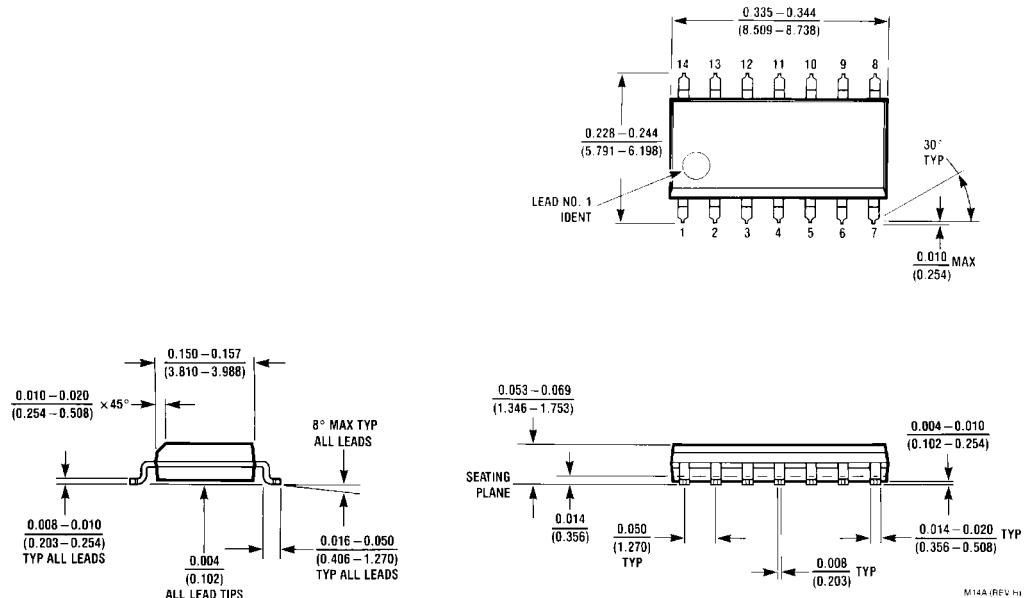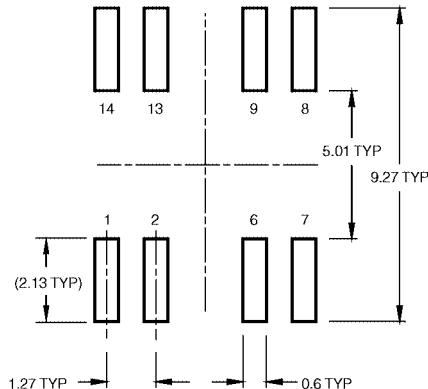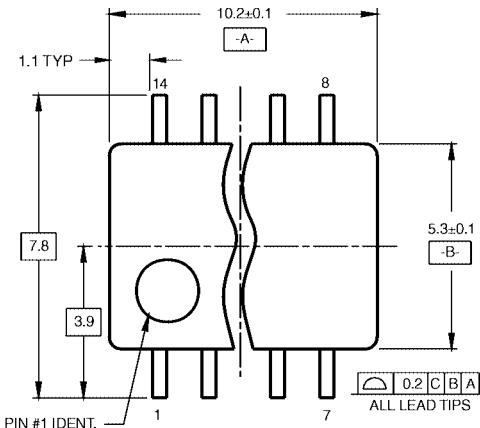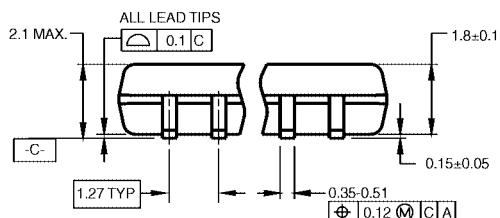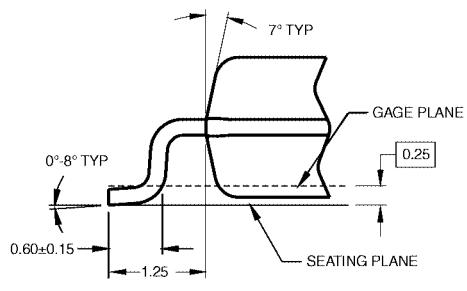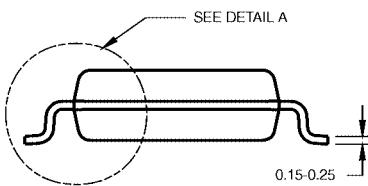
Gate Transfer Characteristics

Propagation Delay vs. Ambient Temperature

Power Dissipation vs. Frequency

Propagation Delay vs. Ambient Temperature

Propagation Delay Time vs. Load Capacitance

Physical Dimensions inches (millimeters) unless otherwise noted

0.335 − 0.344
(8.509 − 8.738)

14 13 12 11 10 9 8

0.228 − 0.244
(5.791 − 6.198)

LEAD NO. 1
IDENT

1 2 3 4 5 6 7

30°
TYP

0.010 MAX
(0.254)

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) × 45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP

0.004 − 0.010
(0.102 − 0.254)

0.014 − 0.020
(0.356 − 0.508) TYP

M14A (REV H)

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

www.sycelectronica.com.ar

SEMICONDUCTORES Y COMPONENTES

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

10.2±0.1

-A-

1.1 TYP

14

8

7.8

5.3±0.1

-B-

3.9

0.2 C B A
ALL LEAD TIPS

PIN #1 IDENT.

1

7

LAND PATTERN RECOMMENDATION

14   13   9   8

5.01 TYP

9.27 TYP

1   2   6   7

(2.13 TYP)

1.27 TYP

0.6 TYP

ALL LEAD TIPS

2.1 MAX.

0.1 C

1.8±0.1

-C-

0.15±0.05

1.27 TYP

0.35-0.51

0.12 (M) C A

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.15-0.25

7° TYP

GAGE PLANE

0°-8° TYP

0.25

0.60±0.15

1.25

SEATING PLANE

DETAIL A

NOTES:
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1
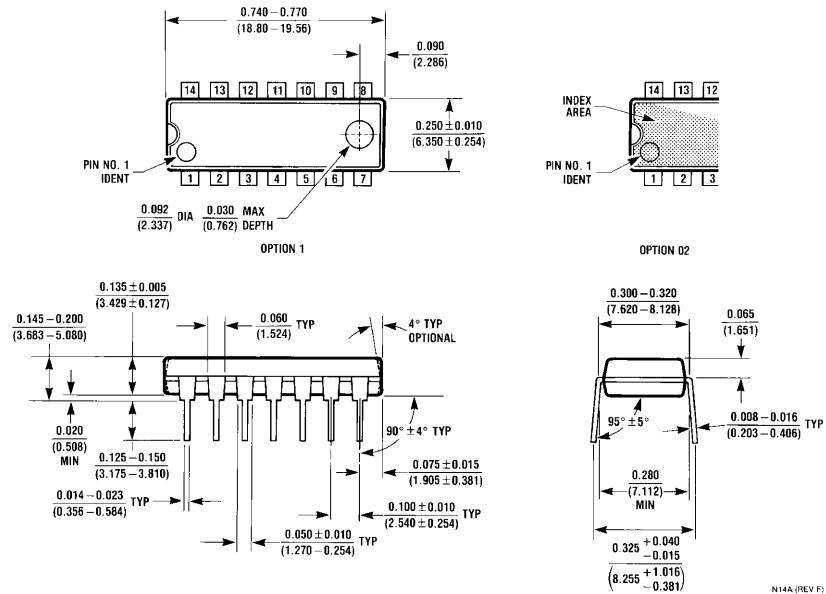
14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.740 – 0.770
(18.80 – 19.56)

0.090
(2.286)

14 13 12 11 10 9 8

0.250 ± 0.010
(6.350 ± 0.254)

PIN NO. 1
IDENT

1 2 3 4 5 6 7

0.092
(2.337) DIA   0.030
(0.762) MAX
DEPTH

OPTION 1

INDEX
AREA

14 13 12

PIN NO. 1
IDENT

1 2 3

OPTION 02

0.135 ± 0.005
(3.429 ± 0.127)

0.145 – 0.200
(3.683 – 5.080)

0.060 TYP
(1.524)

4° TYP
OPTIONAL

0.020
(0.508)
MIN

0.125 – 0.150
(3.175 – 3.810)

90° ± 4° TYP

0.075 ± 0.015
(1.905 ± 0.381)

0.014 – 0.023
(0.356 – 0.584) TYP

0.100 ± 0.010
(2.540 ± 0.254) TYP

0.050 ± 0.010
(1.270 – 0.254) TYP

0.300 – 0.320
(7.620 – 8.128)

0.065
(1.651)

95° ± 5°

0.008 – 0.016
(0.203 – 0.406) TYP

0.280
(7.112)
MIN

$0.325 \begin{smallmatrix} +0.040 \\ -0.015 \end{smallmatrix}$

$\left(8.255 \begin{smallmatrix} +1.016 \\ -0.381 \end{smallmatrix} \right)$

N14A (REV F)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A