AN-5011

Fairchild Semiconductor
Application Note

FAIRCHILD SEMICONDUCTOR™

Low Voltage 3-STATE Power-Up and Power-Down Circuitry

INTRODUCTION

Fairchild Semiconductor's *CROSSVOLT*™ Low Voltage Logic families (LVT, LCX & VCX series) contain circuitry designed to protect both the device and the system they are used in during device power-up and power-down.

This feature is important in applications where there is a requirement to exchange modules while the supply voltage remains on. This circuitry also provides other benefits to system design.

HIGH IMPEDANCE POWER-UP AND POWER-DOWN CIRCUIT USE

The power-up high impedance circuit is especially important in systems where live insertion of boards takes place. By placing the device in a high impedance mode during power up, the device will not send signals onto the data bus until the proper operating voltage level is reached. The device can then correctly receive and send valid data signals. Bus contention, signal glitching, voltage-level degradation, and potential device and system damage are avoided.

Systems that do not need hot insertion capability still benefit from the power-up and power-down high impedance feature. The circuitry protects system components that have different power up ramp rates by preventing a device that has reached its operational level from driving a device or data bus that has not reached operational level. This protects against over voltage damage to device inputs and outputs, as well as bus contention during power up and down cycles. Additionally, it will help prevent false signaling until proper operating voltage levels are reached.

To ensure that the outputs stay in a high impedance state until full operating V_{CC} is reached, it is recommended that a pull up resistor be used to tie the Output Enable pin (OE) to V_{CC} (Note 1). This will keep the device in 3-STATE until the OE pin receives a valid input control signal. Thus, power up and power down voltage-level protection is raised to system operating level.

Note 1: For active LOW enable. For active HIGH enable, a pull-down resistor to ground is recommended.

THE POWER-UP AND POWER-DOWN CIRCUIT

The power-up/power-down circuit is designed to keep the device outputs in a high impedance no-drive state (also known as 3-STATE) during the time the device is ramping up to operating voltage. This function is also activated during the power down cycle. Internal circuitry holds the output enable (OE) circuit in 3-STATE until a predetermined voltage level is reached.

The power-up and power-down circuit consists of a voltage divider network between device V_{CC} and ground. The center tap of the voltage divider is tied to the gate of an NMOS transistor. The drain of the NMOS is connected to the device OE circuit, and to V_{CC} through a resistor. The NMOS source is connected to the device ground plane. With the NMOS device off, the OE circuit is held at the V_{CC} level through the resistor, and the device stays in 3-STATE. When the voltage on the gate reaches NMOS turn on, the voltage level across the drain drops to ground potential, turning off the OE circuit.

Each of the *CROSSVOLT* series has a different high impedance power-up and power-down voltage level. The LVT series has a specified power-up and power-down high impedance of 1.5V and below. The LCX and VCX families are typically in a power-up and power-down high impedance state below 0.8V.

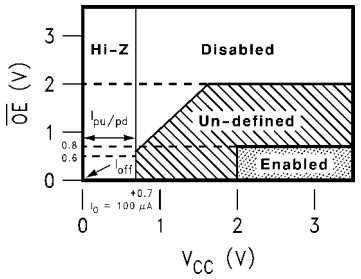

FIGURE 1. Power-up/power-down State Diagram

CROSSVOLT™ is a trademark of Fairchild Semiconductor Corporation.

OVER VOLTAGE TOLERANCE

An additional protection feature of the LVT, LCX, and VCX series is Over-Voltage Tolerance (OVT). OVT gives added protection to these devices during power-up and power-down cycles, as well as during normal operation. The protection consists of an electrostatic discharge (ESD) circuit on the input that does not use the conventional design of a diode between the input and V_{CC}. The *CROSSVOLT* design uses an NMOS device with the gate tied to ground. This provides the high current and voltage protection needed in the case of an ESD event, but eliminates a current path to the V_{CC} rail during over-voltage events. Therefore, the design provides the ESD protection needed, while including over-voltage tolerance.

On the outputs of the LCX and VCX series devices, the PMOS device P5 has its bulk potential supplied by the output of comparator X1 rather than V_{CC} (see Figure 2).

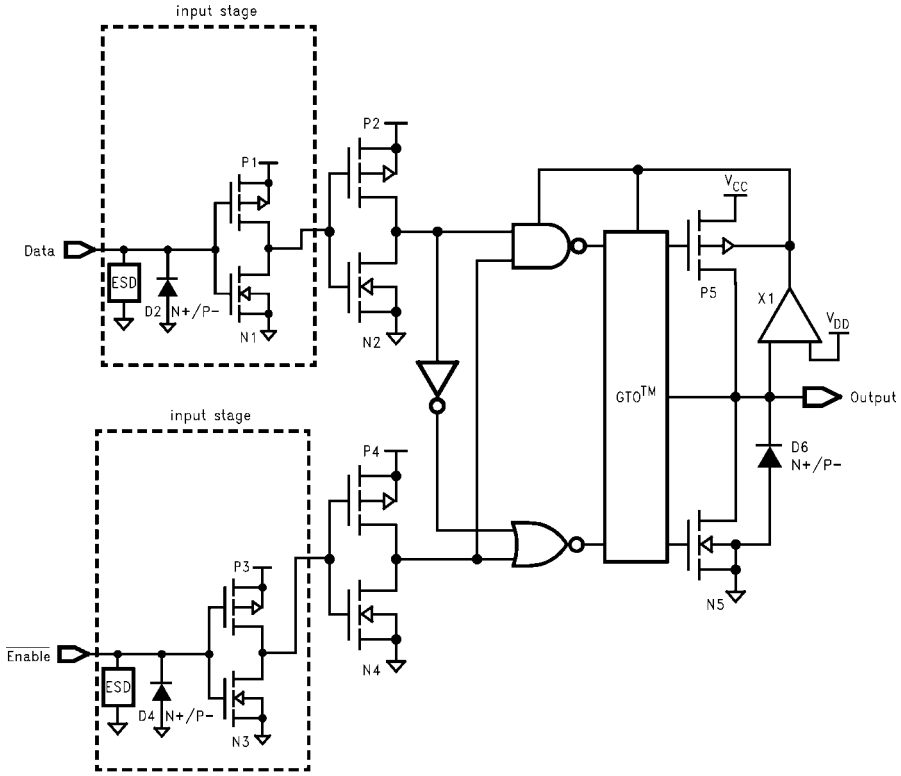

FIGURE 2. Simplified LCX and VCX Schematic Diagram

The comparator is designed so that the output is always the greater of V_{CC} or V_{OUT}. This avoids the P+/N- bulk-source forward junction that appears between the PMOS drain at the output, and the bulk connection of the PMOS that is tied to V_{CC} in more conventional CMOS designs. The design of this junction eliminates a direct current path from the output pin to V_{CC} during over-voltage events.

On the outputs of the LVT series devices, the PMOS device P5 has its bulk potential supplied by the output of comparator X1 rather than V_{CC} (see Figure 3)

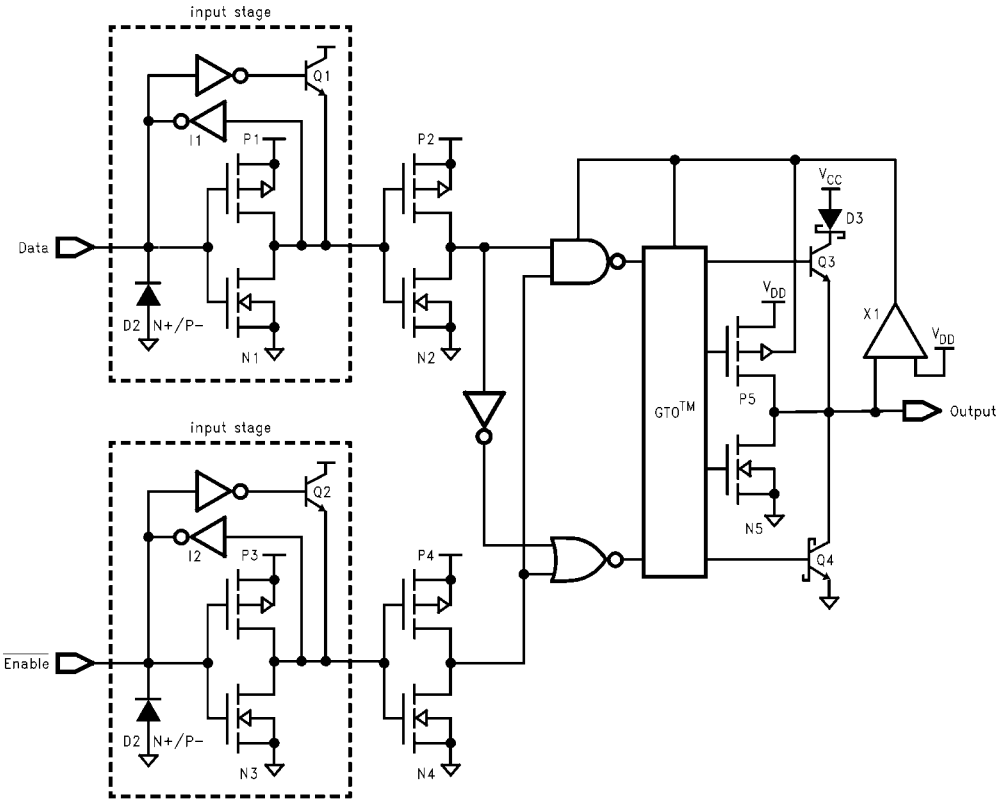

FIGURE 3. Simplified LVT Schematic Diagram

The output circuit design is based upon the LCX circuit and is similar to the over-voltage tolerance design. In addition to the comparator that controls the voltage potential on the base of output PMOS P5, the output includes a reverse-biased Shottky device D3 that prevents output over-voltages in excess of BVCEO from corrupting the low voltage supply.

The same circuit design that provides OVT during powered operation also provides protection to the device during its powered down state, also known as powered down high impedance. This protection is specified as I_{OFF}, also known as Powered Off Leakage Current. The circuitry prevents the device from being powered up through the input or output pins. This protects the device, and potentially, the system from damage or false signaling (See Figure 1).

DESIGN CONSIDERATIONS

When using devices with power up and down high impedance, there are some operational and system design issues that must be considered.

One design consideration is the effect of the power-up and power-down high impedance circuitry on the actual operating voltage of the device. In order to ensure that the device meets the power-up and power-down guaranteed specification across the full temperature range, the actual point of enable and disable during power up and down may be significantly higher than the guaranteed minimum voltage level. In all cases, this level will be less than the guaranteed operating voltage range of the device.

It also must be understood that power-up and power-down high impedance is just one element of what a system needs in order to be completely live insertion protected. While high impedance power-up and power-down helps to maintain a high impedance connection during power cycles, as well as minimize signal glitching and bus contention, it is not a foolproof stand-alone solution to a fault-tolerant, live-insertion system. There are other factors that need to be taken into consideration when designing a system with full live insertion protection.

Module edge connections should be designed to insure the ground pin connects first, with V_{CC} and control pins second, and clock and data pins following. System power management must be designed to insure that V_{CC} droop and current starvation does not occur when modules are plugged into the active system. These are just two of the design concerns for a fault tolerant, fully live insertion capable system.

Summary

Devices designed with power-up and power-down high impedance provide system and device protection, during power up and power down cycles. By isolation of the outputs, signal glitches and bus contention are prevented. This makes these devices ideal for modules that will be used for live insertion.

The design can also protect system devices that have differing power-up and power-down ramp rates by helping to keep outputs from driving signals until all the devices have reached operating voltage levels. To ensure that devices stay in 3-STATE until the full system operational voltage level is reached, a pull up resistor should be connected between V_{CC} and the OE pin.

In addition to the high impedance power up and down feature, the LVT, LCX and VCX series also have Over Voltage Tolerance on the inputs and outputs. OVT protects the device, as well as preventing potential damage to the system. This capability also makes them suitable for voltage translation.

These devices can be of significant help in system protection and proper operation. However, it is important to keep in mind that power-up and power-down high impedance is not all that is needed for a complete, fault-tolerant live insertion system.